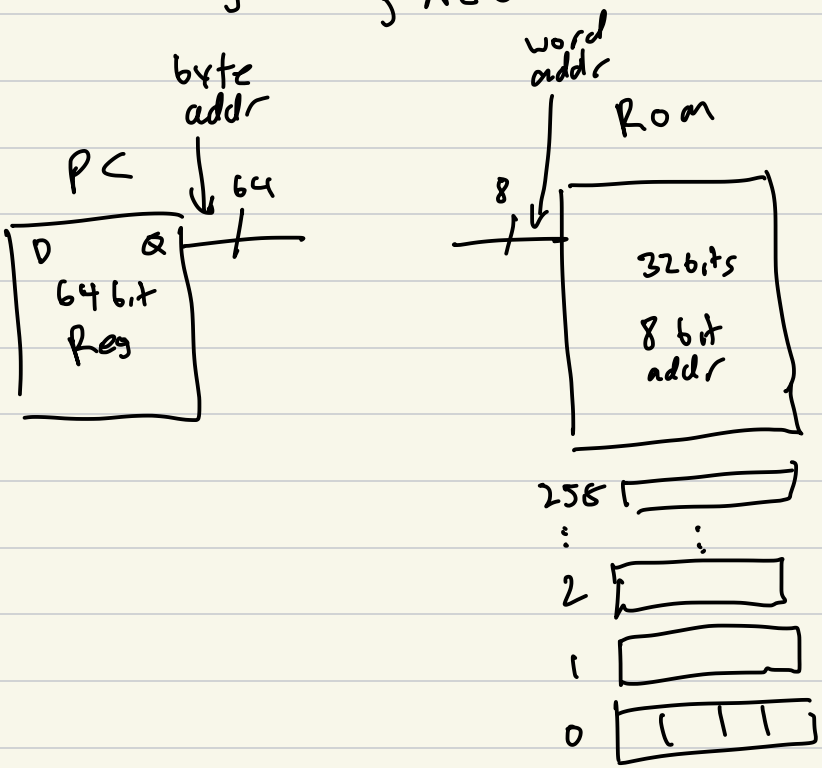
CS315-02 Processor Decoding

Lab05 - RegFile, ALU

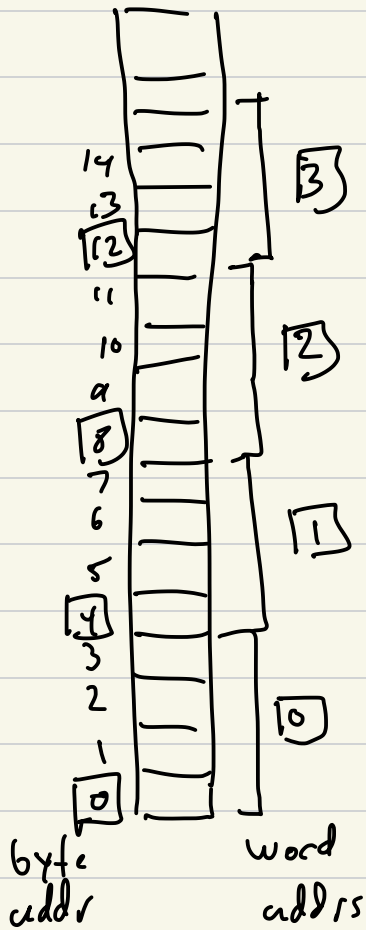


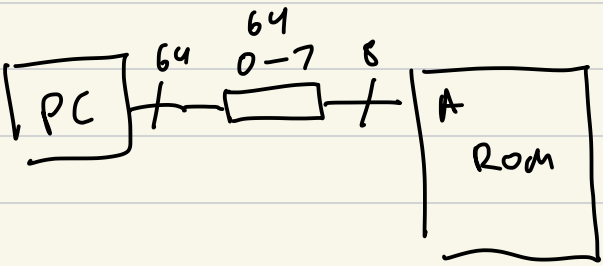
word_addr = byte_addr / 4

word_addr = byte_addr >> 2

8 bit addr means the Rom can hold $2^8 = 256$ instruction words

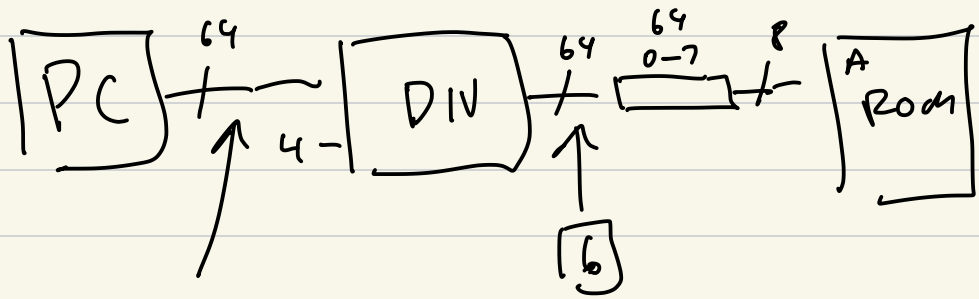
Memory


14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
3
2
1
0
byte addr
word addrs


64
64
0-7
8
PC
A
ROM

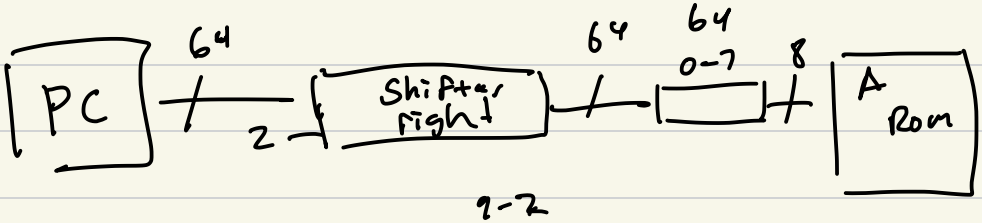
byte addr to word addr

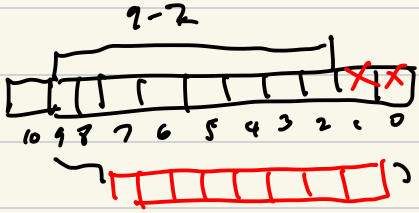
(1)



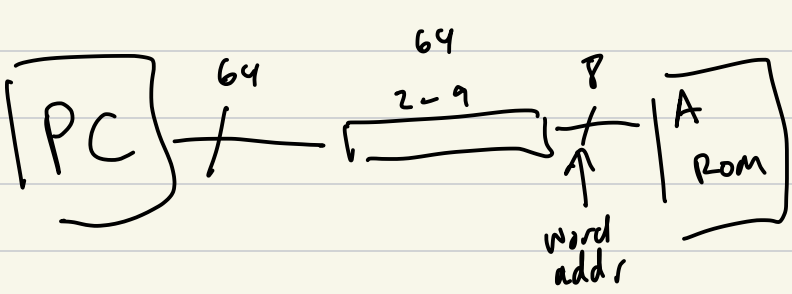
$24/4 = 6$

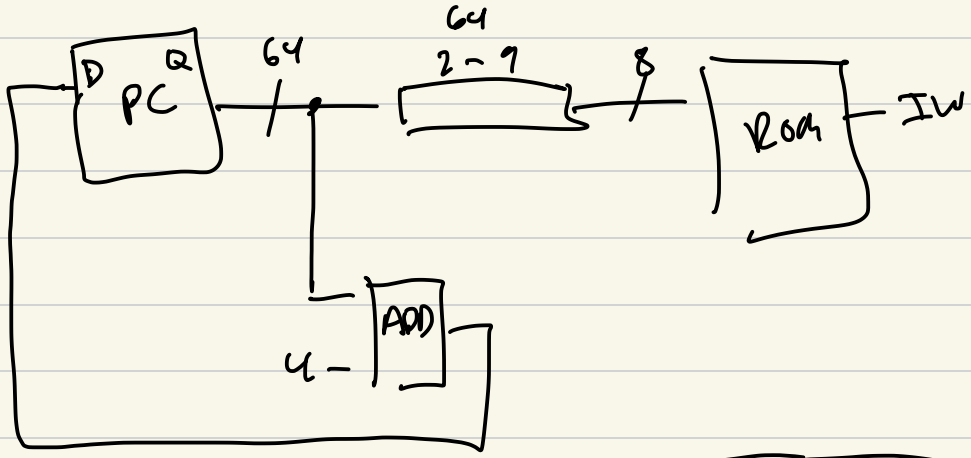
(2)

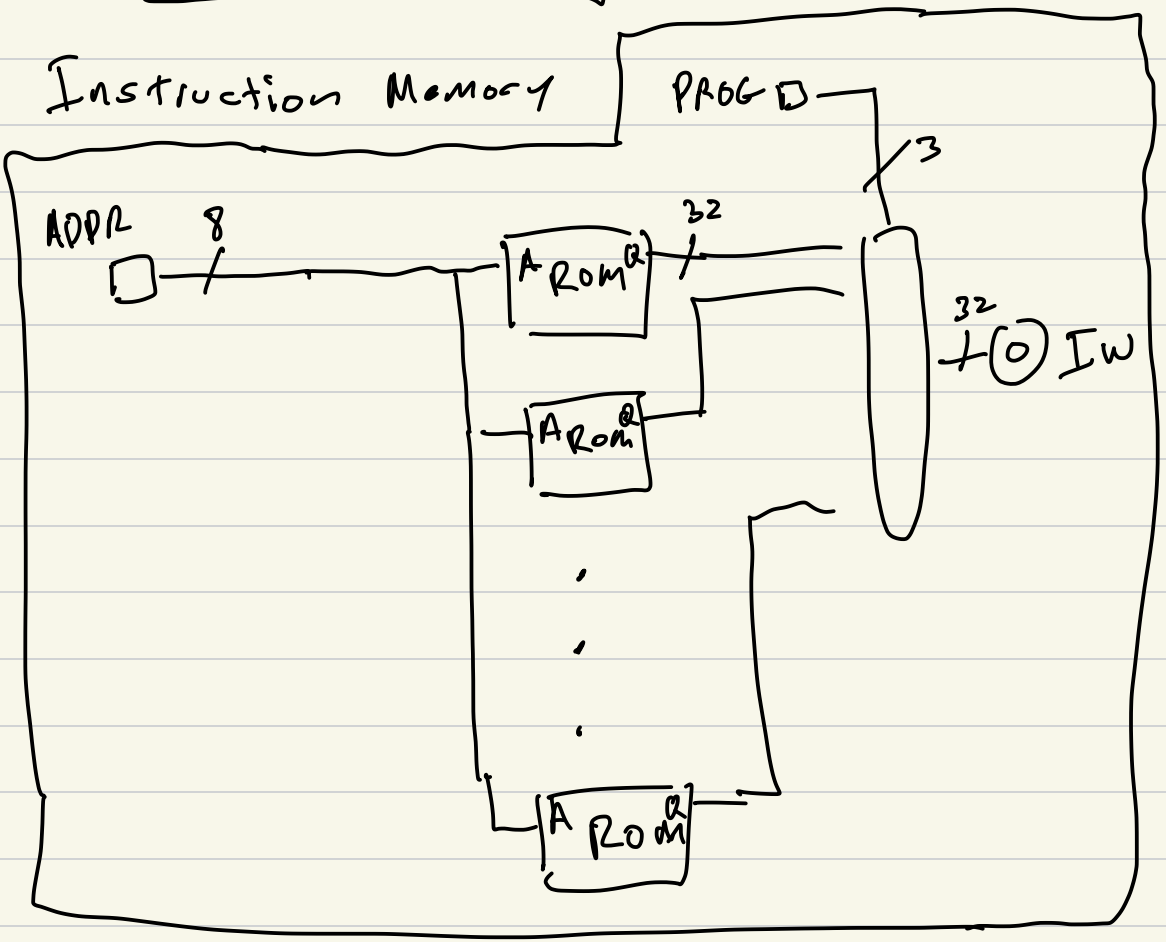




(3)



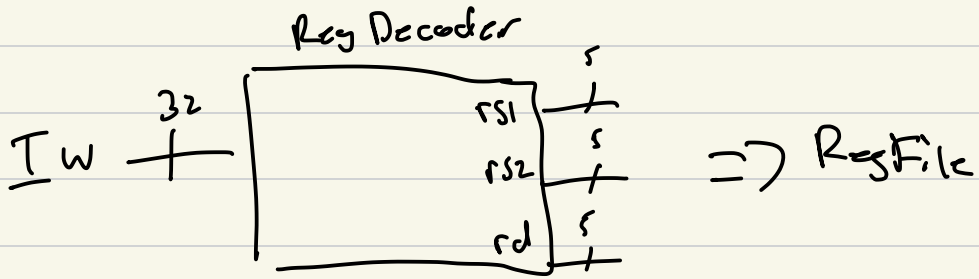

D
Q
PC
64
64
2 - 1
8
ROM
IW
ADD
4 -


Instruction Memory
PROG
3
ADDR
8
32
A
ROM
Q
32
IW

Decoding

RegDecoder
ImmDecoder
InstDecoder

RegDecoder



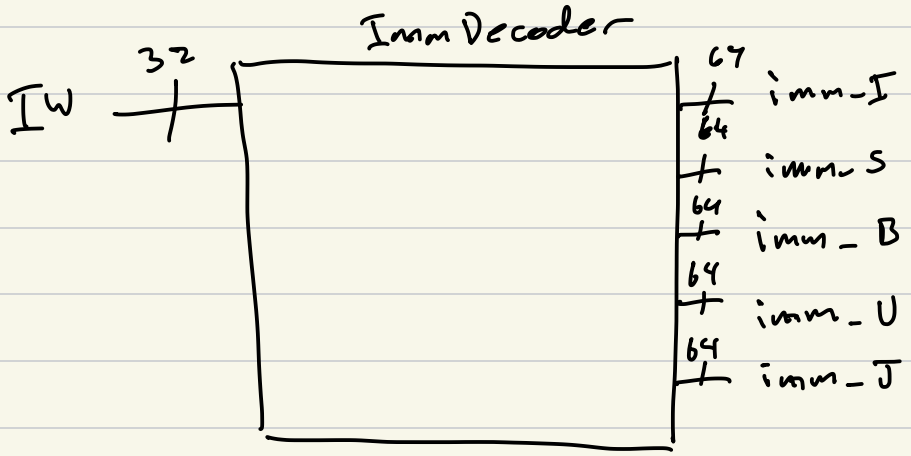
hint: one splitter

add t0, t1, t2

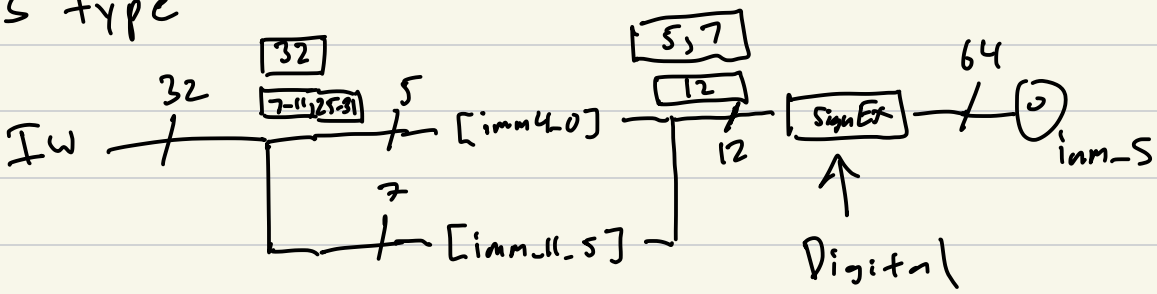
rs1 rs2

RR0 RR1

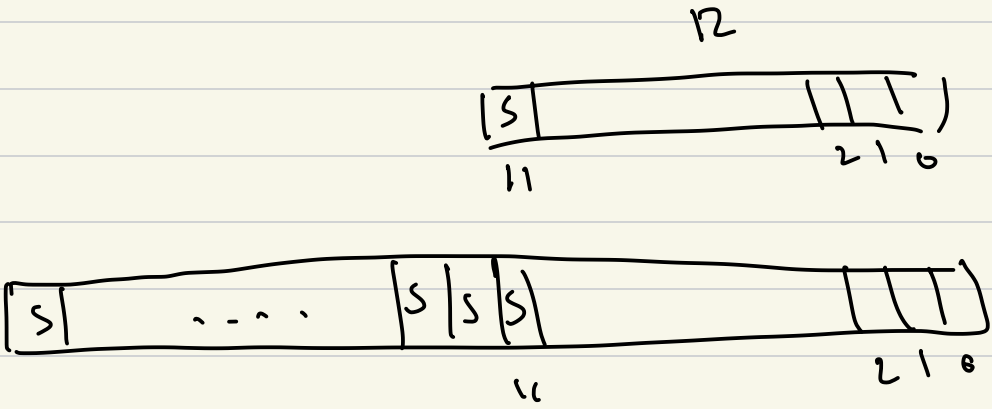
Imm Decoder

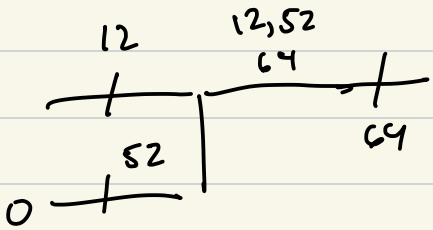


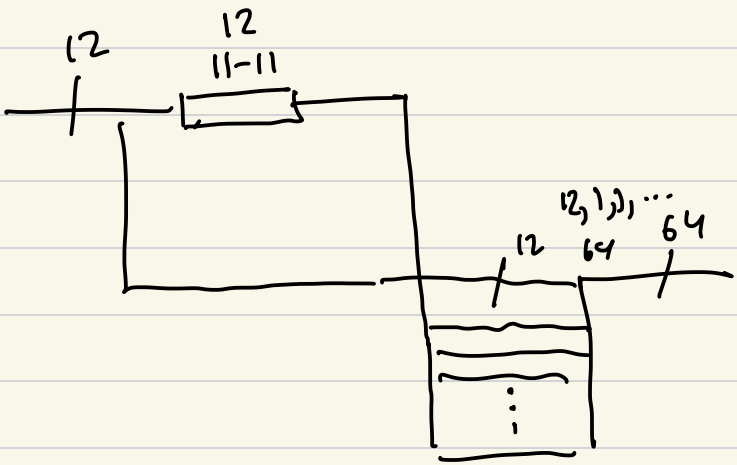
S type

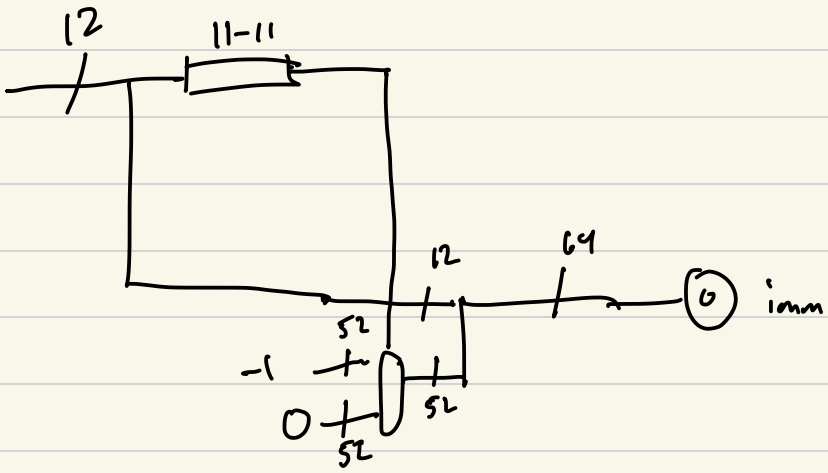


How to implement sign extender with a splitter








12
11-11
12
64
imm
52
-1
52
0
52